CLAIMS

1. A charge pump circuit comprising:

a voltage increasing stage (1);

a voltage decreasing stage (2) in parallel with the voltage increasing stage; and

a shared input (8) to the voltage increasing and voltage decreasing stages.

2. A circuit as claimed in claim 1, wherein the voltage increasing stage (1) is for increasing an input voltage by an integer multiple of the difference between a low supply line voltage (V_{ss}) and a high supply line voltage (V_{DD}) and the voltage decreasing stage is for decreasing an input voltage by an integer multiple of the difference between a low supply line voltage (V_{SS}) and a high supply line voltage (V_{DD}).

3. A circuit as claimed in claim 1 or 2, wherein the voltage increasing stage comprises at least one charge pump section.

4. A circuit as claimed in claim 3, wherein the voltage increasing stage (1) comprises a plurality of charge pump sections, each for increasing the input voltage by the difference between a low supply line voltage and a high supply line voltage.

5. A circuit as claimed in any one of claims 1 to 3, wherein the voltage decreasing stage (2) comprises at least one charge pump section.

6. A circuit as claimed in claim 5, wherein the voltage decreasing stage comprises a plurality of charge pump sections, each for decreasing the input voltage by the difference between a low supply line voltage and a high supply line voltage.

7. A circuit as claimed in any one of claims 3 to 6, wherein the or each charge pump section of the voltage increasing stage (1) and of the voltage decreasing stage (2) comprises an input switch (S_{1A}; S_{2A}) and an output switch (S_{1B}; S_{2B}) in series connected together at a junction node, and a charge pump capacitor (C_{P1}; C_{P2}) connected between junction node and a control line (4;6).

8. A circuit as claimed in claim 7, wherein the or each charge pump section of the voltage increasing stage (1) and of the voltage decreasing stage (2) comprises a first input switch and output switch in series (N1a, P1a; P2a, N2a) connected together at a first junction node, a second input switch and output switch in series (N1b, P1b; P2b, N2b) connected together at a second junction node, a first charge pump capacitor (Cp1a;Cp2a) connected between the first junction node and a first control line (Φ) and a second charge pump capacitor (Cp1b;Cp2b) connected between the second junction node and a second control line (/Φ).

9. A circuit as claimed in claim 8, wherein complementary signals are applied to the first (Φ) and second (/Φ) control lines.

10. A circuit as claimed in Claim 8, wherein non-overlapping signals are applied to the first (Φ) and second (/Φ) control lines.

11. A circuit as claimed in claim 7, wherein the or each charge pump section of the voltage increasing stage (1) and of the voltage decreasing stage (2) comprises a first input switch and output switch in series (N1a,P1; P2a, N2) connected together at a first junction node, and a second input switch (N1b;P2b) connected between the input and a second junction node, a first charge pump capacitor (Cp1;Cp2) connected between the first junction node and a first control line and a second capacitor (Cbs1;Cbs2) connected between the second junction node and a second control line, wherein the

second junction node provides the control signals for the first input and output switches.

12. A circuit as claimed in claim 11, wherein complementary signals are applied to the first and second control lines.

13. A circuit as claimed in claim 11, wherein non-overlapping signals are applied to the first and second control lines.

14. A circuit as claimed in any one of claims 8 to 12, wherein the first input switch and output switch (N1a,P1; P2a,N2) are operated in complementary manner.

15. A circuit as claimed in any one of claims 8 to 14, wherein the charge pump capacitor of at least one charge pump section of the voltage increasing stage and the capacitor of at least one charge pump section of the voltage decreasing stage are connected together.

16. A circuit as claimed in any preceding claim, wherein the voltage increasing stage (1) is for increasing an input voltage by an integer multiple of the difference between a low supply line voltage and a high supply line voltage, the voltage decreasing stage (2) is for decreasing an input voltage by an integer multiple of the difference between a low supply line voltage and a high supply line voltage and wherein a voltage (Vin) is applied to the shared input (8) between the low supply line voltage and the high supply line voltage.

17. An electronic device (30) including a circuit (34) as claimed in any one of the preceding claims.

18. A device as claimed in claim 17, wherein the device (30) comprises a liquid crystal display.

19. A device as claimed in claim 18, wherein the circuit (34) and a TFT switching array (32) for the display are provided on a common substrate (36).